Amendments to the Claims

This listing of claims below will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein a first interconnect of said set of interconnects has a first length, a second interconnect of said set of interconnects has a second length, and said first length and said second length are substantially ~~equal.~~ equal;

wherein said first interconnect is configured to convey a first bit of a number of bits and said second interconnect is configured to convey a second bit of said number of bits.

2. (Original) The cross link multiplexer bus of claim 1, wherein said plurality of cross link multiplexers are arranged in a substantially circular configuration.

3. (Original) The cross link multiplexer bus of claim 1, wherein said plurality of cross link multiplexers are arranged in a substantially spherical configuration.

4. (Original) The cross link multiplexer bus of claim 1, wherein a cross link multiplexer of said plurality of cross link multiplexers comprises a cross link multiplexer pair.

5. (Currently Amended) The cross link multiplexer bus of claim 1, wherein:

said signal is ~~capable of being~~ configured to be represented as a series of characters, and a character of said series of characters is ~~capable of being~~ configured to be represented as ~~a~~ said number of ~~bits; and~~ bits.

~~said first interconnect is configured to convey a first bit of said number of bits and said second interconnect is configured to convey a second bit of said number of bits.~~

6. (Currently Amended) The cross link multiplexer of claim ~~5~~ 1, wherein said first bit remains substantially synchronized with said second bit.

7. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal, at least one delay buffer configured to delay conveyance of said signal, and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link ~~multiplexers.~~ multiplexers;

wherein an interconnect of said set of interconnects is configured to convey a first bit of a number of bits and a delay buffer of said at least one delay buffer is configured to convey said first bit.

8. (Currently Amended) The cross link multiplexer of claim 7, wherein:

said signal is ~~capable of being~~ configured to be represented as a series of characters, and a character of said series of characters is ~~capable of being~~ configured to be represented as ~~a~~ said number of ~~bits;~~ bits.

~~an interconnect of said set of interconnects is configured to convey a first bit of said number of bits; and~~

~~a delay buffer of said at least one delay buffer is configured to convey said first bit.~~

9. (Currently Amended) The cross link multiplexer bus of claim ~~8~~ 1, wherein said delay buffer is one of a series of delay buffers.

10. (Currently Amended) The cross link multiplexer bus of claim 9, wherein said series of delay buffers is ~~capable of conveying~~ configured to convey said first bit through said delay buffer and is ~~capable of bypassing~~ configured to bypass said first bit around said delay buffer.

11. (Currently Amended) The cross link multiplexer bus of claim 10, wherein said cross link multiplexer has a control circuit, said control circuit ~~capable of aligning~~ configured to align said series of delay buffers to be ~~capable of one of conveying~~ configured one of to convey

said first bit through said delay buffer and ~~bypassing~~ to bypass said first bit around said delay buffer.

12. (Original) The cross link multiplexer of claim 11, wherein said control circuit is configured to align said series of delay buffers so that said first bit remains substantially synchronized with a second bit of said number of bits.

13. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a first cross link multiplexer with a destination port configured to receive a signal and a second cross link multiplexer with an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein said first cross link multiplexer is configured to convey said signal toward said second cross link multiplexer in a first direction via a first interconnect of said plurality of interconnects and said first cross link multiplexer is configured to convey said signal toward said second cross link multiplexer in a second direction via a second interconnect of said plurality of interconnects, said first direction different from said second direction.

14. (Original) The cross link multiplexer bus of claim 13, wherein said plurality of cross link multiplexers has a third cross link multiplexer, said third cross link multiplexer adjacent in said first direction to said first cross link multiplexer.

15. (Original) The cross link multiplexer bus of claim 14, wherein said third cross link multiplexer is configured to convey said signal toward said second cross link multiplexer.

16. (Original) The cross link multiplexer bus of claim 13, wherein said plurality of cross link multiplexers has a third cross link multiplexer, said third cross link multiplexer adjacent to said second multiplexer, said second cross link multiplexer configured to receive said signal from said third cross link multiplexer.

17. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein said signal is ~~capable of being~~ configured to be represented as a series of characters, and a character of said series of characters is capable ~~of being~~ configured to be represented as a number of bits;

wherein at least one of said plurality of cross link multiplexers and said plurality of interconnects is configured so that a first bit of said number of bits remains substantially synchronized with a second bit of said number of bits.

18. (Original) The cross link multiplexer bus of claim 17, wherein:

said plurality of cross link multiplexers is configured to delay conveyance of said first bit by a gate delay time;

said plurality of interconnects is configured to delay conveyance of said second bit by a path delay time;

said gate delay time and said path delay time are set so that said first bit remains substantially synchronized with said second bit.

19. (Original) The cross link multiplexer bus of claim 17, wherein a first cross link multiplexer of said plurality of cross link multiplexers is configured to process said signal formatted according to a first physical layer communications protocol and a second cross link multiplexer of said plurality of cross link multiplexers is configured to process said signal formatted according to a second physical layer communications protocol.

20. (Original) The cross link multiplexer bus of claim 19, wherein said first physical layer communications protocol is a 10 Gigabit Media Independent Interface protocol.

21. (Original) The cross link multiplexer bus of claim 19, wherein said second physical layer communications protocol is a 10 Gigabit Attachment Unit Interface protocol.

22. (Original) The cross link multiplexer bus of claim 19, wherein said second physical layer communications protocol is a Converged Data Link protocol.

23. (Original) The cross link multiplexer bus of claim 19, wherein said first cross link multiplexer is configured to reformat said signal formatted according to said first physical layer communications protocol.

24. (Currently Amended) A method for conveying a signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying the signal from a first cross link multiplexer of the cross link multiplexer bus in a first direction toward a second cross link multiplexer of the cross link multiplexer bus; and

(2) conveying the signal from the first cross link multiplexer in a second direction toward the second cross link ~~multiplexer.~~ multiplexer, the first direction different from the second direction.

25. (Original) The method of claim 24, further comprising the step of:

(3) receiving the signal at the first cross link multiplexer.

26. (Original) The method of claim 24, further comprising the step of:

(3) receiving the signal from the first cross link multiplexer in the first direction at a third cross link multiplexer of the cross link multiplexer bus.

27. (Original) The method of claim 26, further comprising the step of:

(4) conveying the signal from the third cross link multiplexer in the first direction toward the second cross link multiplexer.

28. (Original) The method of claim 24, further comprising the step of:

(3) receiving the signal at the second cross link multiplexer from a third cross link multiplexer of the cross link multiplexer bus.

29. (Original) The method of claim 24, further comprising the step of:

(3) transmitting the signal from the second cross link multiplexer.

30. (Original) A method for conveying, in parallel, bits of a character of a signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying a first bit of the bits from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer bus;

(2) conveying a second bit of the bits from the first cross link multiplexer to the second cross link multiplexer; and

(3) delaying said conveyance of the first bit so that the first bit remains substantially synchronized with the second bit.

31. (Original) The method of claim 30, wherein said delaying step comprises the step of conveying the first bit through a delay buffer.

32. (Original) A method for conveying a signal across a cross link multiplexer bus, comprising the steps of:

(1) conveying the signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer bus; and

(2) at one of the first cross link multiplexer and the second cross link multiplexer, converting the signal from a first format to a second format.

33. (Original) The method of claim 32, further comprising the step of:

(3) receiving the signal at the first cross link multiplexer.

34. (Original) The method of claim 32, further comprising the step of:

(3) reconverting the signal from the second format to the first format.

35. (Original) The method of claim 32, further comprising the step of:

(3) transmitting the signal from the second cross link multiplexer.

36. (Original) The method of claim 32, further comprising the step of:

(4) synchronizing bits of a character of the signal.

37. (Original) The method of claim 36, wherein said synchronizing step comprises the step of conveying each bit of the bits through a corresponding delay flip-flop.

38. (Original) The method of claim 37, wherein said synchronizing step further comprises the step of conveying a bit of the bits through a delay buffer.

39. (Currently Amended) The method of claim 32, wherein:

the signal is ~~capable of being~~ configured to be represented as a series of characters;

one character of the series of characters is conveyed during one cycle of a clock that controls conveyance of the signal;

the first format has a first number of bits for data for a first character from the series of characters; and

the second format has a second number of bits for data for the first character and data for a second character from the series of characters.

40. (Original) The method of claim 39, wherein said converting step comprises the steps of:

(a) during a first cycle of the clock, conveying the first character from an input of a first interconnect to an output of the first interconnect;

(b) during the first cycle of the clock, conveying the first character from an input of a second interconnect to a delay flip-flop;

(c) during a second cycle of the clock, conveying the second character from the input of the first interconnect to the output of the first interconnect; and

(d) during the second cycle of the clock, conveying the first character from the delay flip-flop to an output of the second interconnect.

41. (Original) In a cross link multiplexer bus configured to convey a signal in which a character is represented by a first bit and a second bit, a method for synchronizing the first bit and the second bit, comprising the steps of:

(1) determining a first time for the first bit to be conveyed via a first interconnect from a first cross link multiplexer to a second cross link multiplexer when a first series of delay buffers is bypassed;

(2) determining a second time for the second bit to be conveyed via a second interconnect from the first cross link multiplexer to the second cross link multiplexer when a second series of delay buffers is bypassed, the second time greater than the first time;

(3) determining a desired delay time for the first bit so that the first bit is synchronized with the second bit; and

(4) aligning the first series of delay buffers to increase the first time by the desired delay time so that the first bit is synchronized with the second bit.

42. (Original) The method of claim 41, wherein said aligning step comprises the step of configuring the first series of delay buffers so that the first bit can be conveyed through a first delay buffer of the first series of delay buffers.

43. (Original) The method of claim 42, wherein said aligning step further comprises the step of configuring the first series of delay buffers so that the first bit can bypass a second delay buffer of the first series of delay buffers.